

VOICE OF THE ENGINEER

## NEW POWER REGULATIONS

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## New power regulations bring power-factor correction to lower-power supplies

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| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
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| $\mathrm{V}_{\mathrm{cc}}(\mathrm{V})$ | 20 |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{FIT}}$ (V) | 200 |  |  |  |  |  |  |
| Sw Freq. $\max (\mathrm{kHz})$ | 500 |  |  |  |  |  | 400 |
| Gate Drive $\pm(A)$ | +1/-4 | +2/-7 |  | +1/-4 | +1/-4 | +2/-7 | +1/-4 |
| $\begin{aligned} & v_{\text {GIIE }} \\ & \text { Clamp (V) } \end{aligned}$ | 10.7 | 10.7 | 14.5 | 10.7 | 10.7 | 10.7 | 10.7 |
| Min. On Time (ns) | Program. 250-3000 |  |  | 750 | Program. 250-3000 |  | 850 |
| Enable Pin | Yes | Yes | Yes | No | Yes | Yes | No |
| Channel | 1 |  |  | 2 | 1 |  | 2 |
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## The grand challenge of employment

The employment situation in the United States took another hit in July, with the Bureau of Labor Statistics reporting a drop of 131,000 in nonfarm-payroll employment. The Bureau reported that 6.6 million have been jobless for 27 weeks or more, and 8.5 million are working part-time despite wanting full-time employment. If there is good news, it's that much of the employment decline represented the layoff of temporary government census workers. Private-sector payroll employment increased 71,000 over the month, with 36,000 of that number representing manufacturing jobs.

As Robert Reich, professor of public policy at the University of CaliforniaBerkeley, notes, however, "We need 125,000 new jobs per month simply to keep up with the growth of the American population seeking jobs." Clearly, a new golden age of manufacturing in the United States is nowhere in sight.
To former Intel executive Andy Grove, that fact is seriously bad news. He contends that a nation's manufacturing prowess is the key to its ability to innovate. Start-ups alone cannot continue a cycle of innovations (Reference 1). Start-ups are wonderful, Grove writes, but what should follow "that mythical moment of creation in the garage" is equally important, as companies learn to scale up to mass production. Scaling, he says, is "necessary to make innovation matter," but, unfortunately, it's no longer happening in the United States. He cites personal experience with failure to scale, pointing out that Intel's hesitancy to expand production of memory chips enabled its offshore competitors to dominate the market.
Grove notes that Intel did not repeat this mistake with microprocessors. To help other US companies avoid the same pitfall, he proposes strong medicine, including taxing the products of
offshore labor, dedicating the proceeds to companies that will scale up their US production facilities, and creating jobs that can absorb the increasing numbers of people entering the US work force.


If-absent Grove's strong medicine, which Congress seems unlikely to soon administer-the manufacturingemployment outlook is bleak, prospects for $E D N$ readers should be considerably better, according to speakers at National Instruments' NIWeek event, which took place this month in Austin, TX. Keynote speaker Michio Kaku, PhD, a theoretical physicist and TV personality, said that the future is bleak for middlemen, agents, tellers, brokers, and anyone performing repetitive tasks but that the future is bright for artists, leaders, creative people, and intellectual workers of the type who attend NIWeek.
During a panel discussion, NI execu-
tives painted a similarly bright picture for engineers. James Truchard, PhD, president, chief executive officer, and co-founder of NI , commented on recent corporate failures, from the tragic BP oil spill to the nearly comical "antennagate" problems of Apple. Such cases, he said, stem from a lack of healthy communication up the chain of com-mand-which can lead to situations in which safety takes a back seat to the bottom line, as in BP's case, or in which aesthetic concerns outweigh performance issues, as in Apple's case. The consensus seems to be that corporations need to foster an environment in which engineers can have a stronger role in challenging the decisions of dysfunctional management.

As Jeff Kodosky, co-founder and fellow at NI, put it, "Engineering is the only solution to the grand challenges we face. Those challenges can be solved only by engineers."

The NI executives aren't seconding Grove's prescription. "I believe the world is flat, and we must compete on a global basis," said Phil Hester, senior vice president for $R \& D$ at the company. And that idea pertains to engineering as well as manufacturing, he added, with the sun never setting on dispersed teams of innovators. Alex Davern, chief financial officer and senior vice president of NI, said that the goal should center on eliminating low-value jobs and on driving investment that increases the standard of living for everyone.
As the various executives explained, there are no shortages of grand challenges for engineers to solve-from perfecting fusion to safely extracting shale gas. Add to that the challenge of providing meaningful employment for laid-off workers who will never become certified LabView programmers. Let the work begin.EDN

> REFERENCE
> 1 Grove, Andy, "How America Can Create Jobs," Bloomberg Businessweek, July 1, 2010, http://bit.ly/bQGEYv.

Contact me at richard.nelson@cancom.com.

## MEET THE GUY that ELIMINATED HIS TEAM'S MANUFACTURING VARIABILITY ISSUES.



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## Handheld $7-\mathrm{GHz}$ spectrum analyzer quickly and easily makes precise measurements

Agilent Technologies has introduced the $100-\mathrm{kHz}$ to $7-\mathrm{GHz}$ (tunable to 9 kHz) N9342C HSA (handheld spectrum analyzer), which targets engineers and technicians who install, maintain, and monitor the performance of RF systems in the field. The new unit provides broader frequency coverage and more features than earlier members of the manufacturer's HSA family. To simplify making quick, accurate, and repeatable measurements under difficult field conditions, the 7.5lb, $12.5 \times 8.15 \times 2.7$-in. N9342C provides user-customizable capabilities.
The instrument targets use in aerospace/ defense, microwave, satellite, wireless-communication, broadcasting, spectrum-regulation, and general-purpose spectrum-analysis applications. Measurements include transmitter and component test, receivingpath signal monitoring, and antenna tuning. RF-environment measurements include band clearance, signal coverage, and interface hunting. A task-planner feature automates routine measurements, reducing test-setup time by $95 \%$, thereby increasing efficiency.
The HSA provides a set of standard, onebutton measurements, including occupied bandwidth and in-channel and adjacentchannel power, which help you to characterize signal quality. The keypad design allows access to most measurement functions with no more than two button presses.
A rugged, fanless design suits the unit for challenging field environments, and an optional three-in-one ergonomic backpack ensures comfort and provides true hands-
free operation. Moreover, with the LCD's automatic brightness adjustment and the keypad's backlight control, you can easily view the instrument's screen and enter measurement parameters by day or night.
You can use free HSA PC software to remotely control the instrument through a USB (Universal Serial Bus)/LAN connection. The device also has a dedicated user key, a customizable frequency and channel table, and frequency and amplitude correction.

Key N9342C options include a built-in 7-GHz tracking generator, a built-in GPS (global-positioning-system) receiver and antenna that provide precise location information, a spectrum monitor with spectrogram record and playback functions, support for the manufacturer's U2000 USB power sensors that offer high-accuracy power measurement to 24 GHz , a user data-sanitization feature for security purposes, an $8-\mathrm{GHz}$ directional antenna that enables users to hunt for interference, and a built-in power connector for an active RF probe that ensures precise in-circuit measurements. The N9342C HSA's US base price is \$11,113; a typical configuration costs \$12,567.
-by Dan
Strassberg

Agilent Technologies, www.agilent.com/ find/n9342C.
> (-) $)$ FEEDBACK LOOP
> "Anybody out there in hardware land care about the user experience? Solve that, and they'll flock to whatever you've got. Where to start? Try the 'on' button."
> -Ski Milburn, in EDN's Talkback section, at http://bit.ly/c5YbhX. Add your comments.

The N9342C handheld spectrum analyzer thrives in rugged environments, such as installing and maintaining an RF system, doing on-site troubleshooting, monitoring the RF environment, or analyzing interference.


## Isolated dual-channel gate driver delivers 4A

Analog Devices' new ADuM3220 isolated dual-channel gatedriver IC provides 2500V isolation and lets you control two FETs or transistors. The device delivers 4A of peak
stage quiescent current is 1.2 mA , and typical output-stage quiescent current is 4.7 mA . The IC provides $2500 \mathrm{~V} / \mu \mathrm{sec}$ com-mon-mode transient immunity and has an overtemperatureshutdown circuit that activates
at a die temperature of $150^{\circ} \mathrm{C}$. UL (Underwriters Labs) UL1577 ratings and CSA (Canadian Standards Association) and European DIN (Deutsches Institut für Normung) approvals are pending.


You can use the ADuM3220 isolated-gate-driver IC to operate FETs and insulated-gate bipolar transistors.
output current. Input voltage ranges from 3.3 to 5 V , and output voltage ranges from 4.5 to 18 V . Both inputs and outputs feature an undervoltage lockout at 2.5 and 4.1 V , respectively.

The default output voltage is OV , and the maximum signalpropagation delay is 62 nsec , with 5 -nsec matching between channels. The unit operates from dc to 1 MHz ; typical input-

> K( Both inputs and out- puts feature an undervoltage lockout at 2.5 and 4.1 V , respectively. Default output voltage is OV .

The device uses the manufacturer's patented iCoupler technology. It has 60-nsec maximum isolator and driver-propagation delay; junction temperature is $125^{\circ} \mathrm{C}$. It comes in an eight-pin SOIC, operates over a -40 to $+125^{\circ} \mathrm{C}$ temperature range, and has a suggested retail price of $\$ 1.84$ (1000).

## -by Paul Rako

Analog Devices,
www.analog.com.

## DILBERT By Scott Adams



LEDs DELIVER HIGH BRIGHTNESS OR HIGH EFFICIENCY FOR OUTDOOR LIGHTING

Outdoor lighting is subject to the same trade-offs in upfront costs versus long-term operating costs as most other capital investments. You can optimize for LED-light output to reduce the number of emitters per lamp and lower the initial cost of the light, or you can optimize for lamp efficacy and go for the long-term lower operating costs through lower power bills.
To let you make that choice, Philips Lumileds has tweaked its Luxeon Rebel ES product line and lets you continue to use the same Rebel ES emitter. At 1000 mA , the new Rebel ES delivers more than 300 lumens at an efficacy of 100 lumens/W. If you choose to go for system efficiency, lower the current to 350 mA , and efficacy can exceed 125 lumens/W. These LEDs target overhead outdoor lighting for streets, roadways, tunnels, and high- and low-bay lighting, with CCTs (correlated color temperatures) centering at 4100 and 5650K.
The devices' typical efficacy is more than 125 lumens/W, and typical light output is more than 300,220 , or 125 lumens at 1000,700 , and 350 mA, respectively. Typical forward voltage is 2.85 to 3.1V. Price is \$3.89 (100) each.-by Margery Conner \Philips Lumileds, www. philipslumileds.com.

## IMEC touts silicon-germanium MEMS, gallium-nitride-on-silicon, and solar-cell technologies

MEC (Interuniversity Microelectronics Center) highlighted the capabilities of its silicon-germanium-on-MEMS (microelectrome-chanical-system)-technology platform at Semicon West last month in San Francisco. It also announced new partners in its gallium-nitride-onsilicon initiative and claims that its researchers have achieved efficiencies as high as $16.3 \%$ for large-area epitaxial solar cells.
The MEMS capability centers on the development of a 15-micron silicon-germanium micromirror and a grating light valve for high-resolution displays. IMEC realized the devices with its generic CMOScompatible MEMS process for the monolithic integration of MEMS devices directly on CMOS metallization. The micromirror, targeting use in display systems, uses an electrostatic actuation mechanism relying on six electrodes. The design enables analog PWM (pulsewidth modulation) instead of the binary-weighted PWM of current MEMS-based micro-
mirrors. IMEC's novel actuation mechanism allows display of a large range of gray-scale values, whereas binary-weighted PWM depends on the number of subframes or bit planes. The use of analog PWM

IMEC's

## large-

area epitaxial solar cells achieve efficiency as great as $16.3 \%$ on high-quality substrates high-quality substrates
and as great as $14.7 \%$ on low-cost substrates.
thus leads to higher response speed, less image-processing hardware, and less memory. Moreover, IMEC implements the analog PWM on the MEMS level instead of on the CMOS level.

The grating light valve employs MEMS-reflection grating and produces bright and dark pixels in a display system. Diffraction of incident light due to electrostatic deflection of
microbeams in suspension over an electrode controls the display system. The display system can modulate the intensity of the diffracted light when you apply an actuation voltage to half of the beams.


## POE computers operate on less than 25.5W

A list of devices running POE (power over Ethernet) usually comprises low-power applications, such as VO|P
(voice-over-Internet Protocol) phones and videocameras. If you need computer access, you'd likely be limited to a terminal-only device because of the low-power
 requirements of POE. Even the recently adopted higher-power version, IEFE 802.3at, limits the power available to individual devices to 25.5 W over Category 5 cable.

The SkinnyBytes POE computers come in 10.1- and 15.6-in. sizes. ited to a terminal requirements of POE. Even the

SkinnyBytes sees an opportunity here for low-power AIO (all-in-one) computers that use less than 25.5 W . The devices target use in classrooms, in which the cost of adding ac outlets and the hazards of daisy-chaining ac power strips can be prohibitive. To minimize power needs, Skinny Bytes computers use solid-state drives, low-power Intel (www-intel.com) Atom processors, and fanless passive cooling.

Prices for the touchscreen-based systems, which include Windows 7, start at $\$ 699$ for the 10.1-in. tablet, and prices for the $15.6-\mathrm{in}$. AIO system start at $\$ 899$.
-by Margery Conner
SkinnyBytes, www.skinnybytes.com.
micron.com), Applied Materials (www.appliedmaterials.com), and Ultratech (www.ultra tech.com) have also joined the IIAP (IMEC Industrial Affiliation Program, www2.imec.be/ content/user/File/iiap_litho.pdf) on gallium-nitride-on-silicon technology. This multipartner R\&D program focuses on the development of gallium-nitride-on-silicon-process and -equipment technologies for manufacturing solid-state lighting, such as LEDs, and next-generation power electronics components on 8-in. silicon wafers. Manufacturers currently build state-of-the-art LED processes on expensive 4 -in. sapphire substrates. Depositing the gal-lium-nitride material on 8-in. silicon substrates could boost the productivity of gallium-nitridebased device-manufacturing processes.

IMEC also announced 70$\mathrm{cm}^{2}$ epitaxial solar cells with efficiency as great as $16.3 \%$ on highly doped, high-quality substrates. Efficiencies reached as much as $14.7 \%$ on large-area, low-cost, UMG (upgraded-metallurgic-grade) multicrystalline silicon substrates, showing the potential for the industrial manufacturing of thin-film epitaxial solar cells.

## -by Rick Nelson

IMEC, www.imec.be.

# Rarely Asked Questions 

Strange stories from the call logs of Analog Devices

## Watch for Those Multiple Clocking Edges!

Q. How can I improve system performance when using multiple clocks?
A. A common problem that arises when using multiple clocks generated from the same source is noise-usually a spur popping out of the noise floor-because the single clock source is multiplied or divided into several versions of the same clock. Skewing the adjacent edges of each clock allows you to reduce the noise spur, or get rid of it completely, depending on the system's timing margin. This phenomenon indicates a time-variant system, in which corruption on the clock signal is related to the location of the interference in the time domain. The location of the interference is fixed, so the degree of clock corruption is proportional to the magnitude of the interference, just like in a linear system.

As an example, let's take two outputs of the AD9516 clock generator. One output, at 100 MHz , is connected to an ADC; the other, at $25 \mathrm{MHz}\left(1 / 4 \times f_{\text {SAMPLL }}\right)$, clocks an FPGA. Rising and falling edges occur on both output clocks at nearly the same time. The result is a coupling effect, because two fast moving, high-bandwidth edges occur every 10 ns instead of one as desired. During this transition period, the noise-intrinsic or extrinsic-must be low, as jitter or noise can only corrupt the ADC's timing when present during the transition region of the clock. Making the edge faster (and hence the threshold region smaller) by increasing the slew rate will inevitably reduce the amount of time

that noise can be present during the threshold period, effectively reducing the amount of rms (root-mean-square) jitter introduced to the system. During the steady-state period of the clockthe high and low levels-the clock noise is irrelevant. Therefore, simply delaying either the 25 MHz or 100 MHz clock will spread them apart in time, moving the location of the interference. In other words, arrange for the transition edges of one clock to happen during the steady-state period of the other clock.

In essence, what is happening here is crosstalk-induced jitter (noise) from one trace to an adjacent trace. If one trace carries a signal, and a nearby parallel trace carries a varying current, a voltage will be induced in the signal trace; if it is a clock signal, the time at which the clock edge occurs will be modulated. This causes problems if these edges are taking place at nearly the same time.

> To Learn More About Clock Distribution

http://dn.hotims.com/27753-101


Contributing Writer Rob Reeder is a senior converter applications engineer working in Analog Devices highspeed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

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## VOICES <br> Mentor's role in IC and system design

n an interview that took place on July 14 at Semicon West, Walden C Rhines, chairman and chief executive officer of Mentor Graphics, addressed the challenges the EDA and semiconductor industries face as geometries shrink, EUV (extreme ultraviolet) arrives, and ICs go 3-D. He also commented on embedded-system design. An excerpt of the interview follows. Read the full interview at www.edn.com/100826pa.

How is Mentor addressing the challenges of 3-D?


We are working directly with customers to ensure that the tools we provide are available ahead of the need. Physical verification is one of the straightforward pieces that people look to us to set standards for. Today, beyond memory, most of the 3-D usage is still pseudo 2-D-that is, stacked memory with logic or memory with analog. You can treat the design as 2-D, so it really hasn't created the big challenges that we have ahead.

## What are the challenges ahead?

AAhead, more and more we will be facing issues with parasitic extraction, timing, and floorplanning.

Are there still issues to address even in the 2-D chips, and does process shrinkage drive those issues?
A It's driven by a couple of things. Manufacturing variability, of course, is a driving force that becomes a bigger percentage of impact on a design with time. But I think the big discontinuity came when an EDA com-
pany-Mentor-was able to correlate the database from test results with the database from physical layout.

Will there be issues with EDA when going to EUV?

AEUV will require resolution enhancement, just as 193-nm immersion does. There is no scenario I know of where it will hit at such a time that you won't require resolution enhancement to go with it.

Is there still more work to be done with the 193 nm ?

AYes, it's a real workhorse light source. If you look [at it] compared to other generations of lasers, we've really stretched 193 nm a long way and will continue to push it, and it's very clear to us that our computational lithography will be able to bear the burden of shrinking to 20 nm .

What about power-aware design?
A It is probably the single biggest challenge of designers today. It clearly supersedes performance and density in terms of being the limiter of new designs. To me, the big opportunity ahead is moving the power analysis earlier in the design phase.


Mentor Graphics has products for embedded-system design. One thing that came out of the Design Automation Conference was the keynote address by the corporate vice president of innovation products at Motorola Mobile Devices Inc, who talked about designing the Droid phone. He said his big problem was that design tools did not let him optimize power, for example, at the end-product level. Are there prospects for addressing that problem?

Yes. So system-level optimization, which involves multiple chips or board-level design, is not only a big opportunity; there are also tools available. First, there are power-integrity tools at the system level available, and one has actually been the fastest-growing systemdesign tool in our history. This year we went from zero to millions of dollars of sales in a period of about six months. So that's one piece. Another is the ability to have an embedded operating system that allows for power optimization. In fact, we have such an embedded operating system, Nucleus, and we have customers who have achieved order-of-magnitude
improvements in power consumption simply by how they did things in the real-time operating system.

## What about combining

 mechanical and EMI (electromagnetic) simulations at the system level, as well?$A$Multiphysics simulation has been a major focus for us for many years now. It's been slow-growing, but it's been quite popular with the systems companies—solving problems, typically in the mechanical, electrical, and optical domains. We provide multiphysics simulation, optimization, and modeling capabilities, and that's a very promising area that's growing rapidly for us.

Within Mentor, do you see a shift in revenue you get from semiconductor products versus system-level products?

I believe that, first of all, we see continued strengthening in system-level products, meaning systemdesign, analysis, embeddedsoftware, thermal-analysis, and other system-level tools. And it will represent a growing share of our total revenue as we move out in time.
-interview conducted and edited by Rick Nelson

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## How voltage references affect mixed-signal parts

You might blame your ADC's or DAC's lack of output stability on the converter itself. After all, these types of devices can be complex. Try not to pass judgment too fast, though, because the circuitry around your converter might be the culprit. This circuitry, which includes a voltage reference, can change the converter's performance more than you may imagine.

In your initial evaluation of your converter, you may not even see the ill effects of your voltage reference. In the past, when evaluating an ADC or a DAC, I would first make sure that the converter's digital interface was in order and check to see whether the converter's output generally represented the input signal. I then looked at the zeroinput converter noise. When you measure the noise of an ADC , you short the inputs and connect close to ground.


With a DAC, you program the digital input to an analog zero output.
Where might you look for an ADC or DAC voltage-reference error? The key to answering this question is in the transfer function of these devices. In Figure 1, the numerator on the right-hand side of these functions has the input signal times $2^{\mathrm{N}}$, where N is the number of converter bits, and the denominator has the magnitude of the voltage reference in volts. The $2^{\mathrm{N}}$ and


Figure $1 D_{\text {OUT }}$ is the decimal representation of ADC's output code, $A_{\text {IN }}$ is the ADC's input voltage, N is the ADC's and DAC's number of bits, $\mathrm{V}_{\text {REF }}$ is the reference voltage in volts, and $D_{\text {IN }}$ is the decimal representation of the DAC's input digital code.
$\mathrm{V}_{\text {REF }}$ values are constant. The impact of the voltage-reference value-and its errors-increases with an increasing input signal.

The best way to analyze and evaluate your data converter's voltage reference is with a full-scale output signal. A voltage reference with an offset error creates an ADC or a DAC gain error. If your voltage reference is noisy or marginally stable, you will also see this noise or instability, which will become worse when the converter's output is close to full-scale.

The analog output of an ADC or the digital results of the DAC can be only as good as the voltage reference in your circuit. When you choose your voltagereference source, consider the following tips.

Using the system power-supply voltage at your converter's voltage-reference pin is a good technique only when dealing with 8 -bit ADCs at best. Consider the origin of the power-supply voltage. For instance, dc/dc or switching converters produce acceptable dc outputs for circuits. However, they usually have an internal switching network that produces noise on the dc signal. Even when you implement lowpass filtering, remnants of the switching action in the dc/dc converter may transmit to the output of your ADC or DAC device. You may also try to follow a dc/ dc or switching converter with a linear regulator. Linear-regulator power-sup-ply-rejection and output noise levels are improving, but you may find that 10-bit devices and those operating at more than 10 bits still have problems.

An even riskier source for your converter's voltage-reference pin is your computer's USB port. The power-supply voltage from your USB port has the computer's digital noise riding on it-a poor environment for these types of devices. For higher-resolution ADCs and DACs, the best strategy is to start your design with a low-noise, stable, standalone reference.EDN

Bonnie Baker is a senior applications engineer at Texas Instruments.

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## Sony Ericsson's Xperia X10 mini: the teardown skinny

High-end smartphones, such as Apple's iPhone series and Google's Nexus One, might capture a disproportionate percentage of industry attention, but plenty of folks just want a handset that will make and take calls, handle e-mail and Web surfing, and fit comfortably into a normal-sized pocket, too. Sony Ericsson's Xperia X10 mini, which the company based on Google's Android operating system, aims to address this market need. Does it succeed? iFixit and EDN decided to find out (see http://bit.ly/bJLJPw).

The diminutive device measures $3.3 \times 2 \times 0.6$ in. and weighs 3.1 oz. It comes in two versions: the conventional variant and a profes-

[^0]sional model that also includes a QWERTY physical keyboard and consequently weighs 1.1 oz more. Both devices leverage a Synaptics ClearPad 2000 capacitive touchscreen and a Samsung 2.6-in. LMS255GF02 QVGA (quarter-video-graphics-array) LCD, whose resolution limitations preclude the installation of some Android Market-sourced applications. A controller IC, also from Synaptics, drives the display. Although it supports two-finger-touch capabilities, the Android Version 1.6 variant currently running on the handset doesn't support multitouch functions. Sony Ericsson plans to offer an Android Version 2.1 upgrade for the entire Xperia X10 line by the end of the year. It also plans a variant of the "mini"-handset hardware design, currently code-named Yendo, with availability forecast by the end of this quarter. This version will dispense with Android and instead harness a Sony Ericssonproprietary operating system.


> The processing nexus of the Xperia X10 mini is Qualcomm's MSM7227 Snapdragon ARM-based chip set (see http://bit. ly/aSxHz5), which the company unveiled in February 2009 . The MSM7227 targets system designs selling for less than $\$ 150 ;$ HTC's HD mini and Legend and Kyocera's Zio M6000 also use the MSM7227. It includes a 600-MHz application processor with a floating-point unit; a 320-MHz application DSP; a 400-MHz modem processor; hardware-accelerated 3-D graphics; integrated Bluetooth Version 2.1 with A2DP (advanced-audio-distribution-profile) capabilities; support for a still-image camera with resolution of as much as 8M pixels; and 30-frame/sec video capture at up to a WVGA (wide-VGA) resolution. This particular hardware design uses a 5M-pixel still-image camera module with VGA-resolution video capture, autofocus, and built-in LED-flash illumination.

The Xperia X10 mini's 2-Gbit NAND-flash memory, only half of which is user-accessible, comes from STMicroelectronics. The chip is a multidie stack; inside the package, you'll find not only the flash memory but also 2 Gbits of DRAM. MicroSD support enables Xperia X10 mini owners to somewhat augment the handset's builtin nonvolatile-memory capacity; the Android operating system currently allows only data storagenot application installation-on removable memory modules.

Qualcomm's chip set also comprises the PM7540 power-management IC and the RTR6285 UMTS (Universal Mobile Telecommunications System) HSPA (high-speed-packet-access) transceiver and AGPS (advanced global-positioning-system) receiver. Cellular-network-support options include GSM, GPRS (general packetradio service), and EDGE (enhanced data rates for global evolution) at 850, 900, 1800, and 1900 MHz ; UMTS HSDPA at 900 and 2100 MHz ; UMTS HSDPA at 850, 1900, and 2100 MHz ; and UMTS HSUPA at 850, 1900, and 2100 MHz .

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MECHATRONICS

## Isn't there enough real inertia around?

Electronic inertia through acceleration feedback improves performance.

The word "inertia" in everyday use suggests resistance to change and an unwillingness to act. Inertia is hardly something you need in engineering practice to solve the urgent problems you face. Even in a motion-system context, the idea of adding inertia, or mechanical mass, to a system is not usually desirable because it slows system response. One familiar exception is adding a flywheel to an engine or a machine to smooth out speed fluctuations. Two of the most important benefits of feedback control are command following and disturbance rejection. The focus of attention in a control system is usually on command following, but the ability of a system to reject disturbances is paramount in many situations.
For a motor-velocity feedback-control system, increasing inertia reduces the high-frequency disturbance response-

## For mechatronics engineers, adding inertia is desirable in one situation.

that is, it makes the system dynamically stiffer at high frequencies. However, it also degrades the closed-loop command following. How do you add inertia without degrading command-following performance?
A common industry motion-control system has cascaded feedback loops for motor current, velocity, and position. Newton's second law states that torque is proportional to angular acceleration. Thus, if you can measure or estimate acceleration, you can scale the acceleration by inertia, J, to give units of torque and then by $1 / \mathrm{K}_{\mathrm{T}}$, the inverse of the mo-tor-torque constant, to give current. You then multiply this


Figure 1 You realize the benefits of acceleration feedback when you scale up controlloop gains by the amount that the inertia increases-that is, by the factor $1+\mathrm{K}_{\text {AFB }}$.
result by a gain, $\mathrm{K}_{\mathrm{AFB}}$, and subtract it from the current command to the current-control loop. $\mathrm{K}_{\text {AFB }}$ has a similar effect in increasing inertia; hence, it has the alternative name "electronic inertia." To ensure that the command-following performance remains the same, you must scale the velocity-control gains by the same factor, $1+\mathrm{K}_{\text {AFB }}$.

The value of $\mathrm{K}_{\text {AFB }}$ does not affect the velocity-command response because the loop gain increases in proportion to the inertia, producing no net effect. So, why add electronic inertia? The real benefit of acceleration feedback is that acceleration feedback through the entire frequency range improves the disturbance


Kevin C Craig, PhD, is the Robert C Greenheck chair in engineering design and a professor of mechanical engineering, College of Engineering, Marquette University. For more mechatronic news, visit mechatronics zone.com. response in proportion to the term $1+\mathrm{K}_{\mathrm{AFB}}$ (Figure 1).

You cannot significantly realize this improvement above the bandwidth of the current loop because the accelerationfeedback signal cannot improve the system at frequencies in which the current loop cannot inject current. These cases require a robust acceleration-feedback signal. You can accomplish such a signal through differentiation of a position sensor signal and filtering or through the use of an observer.

For mechatronics engineers, adding inertia is desirable in one situation. In the virtual world in which we live, you almost expect electronic inertia. Peter Schmidt of Rockwell Automation and Robert Lorenz at the University of Wisconsin-Madison have done foundational work in this area, and you should consult their findings. For additional information, go to http://bit.ly/ adSO1I.EDN

[^1]

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# HARDWARECONIROLIED BRUSHIESS DC MOIORS EASE THE BURDEN ON CPUS 

YOU CAN EMPLOY A HARDWARE-ONLY MOTOR-COMMUTATION SCHEME TO CONTROL MOTOR SPEED, FREEING THE SYSTEM CPU TO PERFORM FUNCTIONS SUCH AS RF COMMUNICATION AND DATA ENCRYPTION.


LDC (brushless dc) motors have replaced other motors in applications ranging from air conditioners to remote-controlled cars, providing advantages in efficiency, reliability, and performance. The cost of BLDC motors has decreased dramatically over the last 10 years, causing their adoption rate to spike.
Controlling a BLDC motor is somewhat straightforward, and most microcontrollers can do it. However, in applications requiring a high revolutions-per-minute rate-for example, textile machines, remote-controlled cars, and industrial controls-the constant highpriority interrupts that increase in frequency as the speed of the motor increases can tax the CPU. That scenario would be OK if motor control were the microcontroller's only function. A better approach is to use a method of hardware-only motor commutation that offloads the CPU from the burden of maintaining a motor's speed, freeing it to perform other functions, such as RF communication, data encryption, or 3-D-position calculations.
When implementing a motor-control design, engineers can choose between fixed-function motor-control ICs and
microcontrollers. In many designs, engineers choose microcontrollers because they provide flexibility and the ability to integrate a variety of other functions from the user interface, such as buttons, switches, and displays, to communication functions, such as UARTs (universal asynchronous receiver/transmitters) and SPIs (serial-peripheral interfaces). However, because of the high quantity and priority of interrupts necessary for controlling the motor, a mo-tor-control microcontroller can implement only slow, non-CPU-intensive peripheral functions. If the end device requires functions such as data encryption, vector analysis, or other types of

CPU-intensive features, you may have to use a faster and more expensive microcontroller or split the design into a dedicated microcontroller for the mo-tor-control portion and another microcontroller for the other functions. This approach costs more in engineering time, board space, and overall BOM (bill-of-materials) expenses. As an alternative, you can employ a method of hardware-only motor control that offloads from the CPU these taxing periodic motor-control interrupts, freeing it to perform other functions and allowing full design integration into a single microcontroller. This method also lets you easily drive multiple motors at dif-

ferent speeds, paving the way for BOMexpense reductions in applications requiring multiple motors that today use multiple dedicated microcontrollers.

To understand why BLDC-motor control is so prone to interruptions, consider how a microcontroller controls it. An electronically controlled BLDC motor requires you to energize the stator windings in a particular sequence (Figure 1). To implement this sequence, the control circuitry must know the rotor position. Sensor-controlled systems use sensors, such as Hall-effect sensors embedded in the motor stator; sensorless-control systems use back EMF (electromotive force). With Hall-effect-sensor-based systems, the rotor's magnetic poles pass near the Hall sensors, supplying a high or a low signal, indicating that the north or the south poles are passing nearby. The exact combination of the three Hall-sensor signals signifies the position of the rotor. Successively energizing stator windings with appropriate north and south poles keeps the motor turning (Figure 2).

A microcontroller rotates the BLDC

## AT A GLANCE

$\boldsymbol{\otimes}$ BLDC (brushless dc) motors provide advantages in efficiency, reliability, and performance and have replaced other motors in a range of applications.
$\boldsymbol{y}$ Engineers can choose between fixed-function motor-control ICs and microcontrollers.

Hardware-only motor commutation offloads from the CPU the burden of maintaining a motor's speed, freeing it to perform other functions, such as RF communication, data encryption, or 3-Dposition calculations.

You can directly map the various functions for controlling a BLDC motor in the resources of a microcontroller, creating hardware-only commutation.
motor by enabling and disabling external power devices that deliver current through the stator windings in the required sequence. Effective commutation requires that you energize the timing of the winding current in sequence
with the rotation of the motor. For control of BLDC motors, a Hall sensor's change of state generates an interrupt, which indicates that the motor has rotated into the next commutation state. At this point, the CPU must determine which PWM (pulse-width-modulated) outputs to enable and disable based on the state it has just entered. The faster the motor is rotating, the more often the CPU interrupt will occur. The commutation-state interrupts must be high priority and have quick service to ensure smooth rotation and to maintain control of the speed of the motor.

Traditional six-step phase commutation requires six microcontroller service interrupts to complete one electrical cycle. Most motors contain multiple pole pairs around the circumference of the stator, requiring multiple electrical cycles and many more interrupts per rotation. This requirement increases the load on the processor and limits the maximum rotation speed.

In contrast, hardware-controlled commutation frees the processor to run other tasks, allows very-high-speed rotation, and enables higher levels of


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Figure 2 Control circuitry energizes windings in the stator to create north and south poles that attract and repel, respectively, south and north poles in the rotor.


Figure 3 With hardware-controlled commutation, motor-control functions map into configurable analog and digital resources that avoid the involvement of the CPU.
integration of system functions into the microcontroller. In this implementation, the commutation functions that
the CPU performs following each interrupt map into configurable analog and digital resources that control motor

rotation without involving the CPU. This step eliminates the interrupts and makes the motor-control function almost autonomous. This method is not possible in some cases. For example, you cannot use it in designs requiring more advanced control algorithms, such as sinusoidal or field-oriented control. Figure 3 shows how you can directly map the various functions for controlling a BLDC motor into the resources of a microcontroller, creating hardware-only commutation.

You implement commutation control with configurable hardware resources, including a PWM, a hardware look-up table, and a hardware over-current-protection block. (You can view a schematic of a hardware-only BLDC-motor-control implementation in the Web version of this article at www.edn.com/100826df.) An integrated ADC measures a desired analog-speed-control input. Traditional designs
execute commutation in firmware.
Input control signals to the hardware blocks include motor-current detection, which uses an analog input pin to detect and cut off the power-device driver to protect the motor when an overcurrent condition occurs. The signals also include three digital input pins that connect to the outputs of the Hall-effect sensors from the motor. These sensors provide the position of the rotor and control the commutation by varying the PWM's output signals to the power driver.
The design has three user-inter-face-control inputs: direction control, which comprises a digital input that connects to a switch to control the motor's clockwise and counterclockwise rotation; start/stop control, which comprises a digital input that connects to a switch to start and stop rotation of the motor; and speed command, an analog input pin that measures the voltage across a potentiometer to set the desired speed of rotation. Outputs from the motor controller include PWM signals to both the high and low sides of the power-device driver.
The circuit generates a PWM reference signal and routes it to a hardware combination-logic block, along with the three Hall-effect-sensor inputs and motor-direction and -enable controls. This logic block, a look-up table using PLD (programmable-logic-device) resources, creates the six PWM-control signals for routing through GPIOs (general-purpose inputs/outputs) to the external power drivers. Figure 4 shows the configuration of the look-up table. A firmware-proportional-integral speed-control loop adjusts the duty cycle of the PWM output. Speed adjustment is the only function of motor control that the CPU needs to be involved in. However, this function is not taxing because the speed-control loop can be run at a much slower rate, and it need not be a high-priority interrupt.
The sequencing of the PWM-control signals to the external power drivers produces motor commutation. The PWM includes dead banding to prevent the enabling of wrong coils at the same time during signal transitions and creating unwanted shoot-through current. A timer with a hardware capture measures the rotation speed. The timer triggers from a rising edge of a Hall sen-
sor, and the rotation speed is stored in a register that the firmware speed-control loop can read when necessary.
You can also fully implement overcurrent detection in hardware for fast and low-cost motor protection (Figure 5). $R_{1}$, a shunt resistor in the ground path of the power-inverter module, measures motor current. This voltage is
level-shifted on the board and connects to the analog input, or current, pin on the microcontroller. The input voltage feeds into an internal PGA (program-mable-gain amplifier) that multiplies the difference between the input voltage and the reference voltage, a buffered voltage at half the analog supply, and connects the output to a compar-


Variety of broadband delay line ICs that feature precise linear analog delay control, output amplitude adjustment, temperature compensation, and low power consumption. They can process data / clock signals from DC up to $40 \mathrm{~Gb} / \mathrm{s} / 32 \mathrm{GHz}$. The delay lines come in either standard 24 -pin plastic QFN or custom high performance 24 -pin metal ceramic packages.

Several SerDes solutions including a digital broadband 16:1/1:16 MUXVDMUX, operating from DC up to 16 GHz; 16:1 MUX CMU and 1:16 CDR DMUX that are Telcordia compliant, operating at $12.5 \mathrm{~Gb} / \mathrm{s}$, housed separately in standard 100 -pin QFN packages. Other ASICs are digital $2: 1$ and 1:2 SerDes pair running at $50 \mathrm{~Gb} / \mathrm{s}$; variety of variable output amplitude limiting amplifiers; Linear TIAs and dual TIAs; Clock/Data Splitters; Frequency Dividers and Glue Logic Components.

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Figure 5 Hardware-implemented overcurrent detection provides fast and low-cost motor protection in a three-phase-motor, highvoltage power-module board (left). A comparator kills the PWM output when a current-detection input voltage is over the currentlimit threshold that the DAC sets (right).
ator. The circuit compares the voltage level to the current limit. An 8 -bit voltage DAC sets the current-limit value in a register and converts it to an analog voltage. The comparator output connects to the hardware kill input of the PWM and kills the PWM output when the current exceeds the limit threshold. This function provides cycle-by-cycle current limiting to the BLDC motor.
To configure overcurrent protection for a desired current limit, you must select values for the resistor and the current-limit threshold. The value of the overcurrent-detection shunt resistor represents a trade-off between head room for the motor operation and robustness of the detection blocks. For a given current limit, the motor current must generate enough change in voltage to accurately detect the change with the comparator. However, increasing the resistor increases the ground voltage of the inverter and reduces the head room to drive the motor.
The current-limit threshold is equal to $\mathrm{R} \times \mathrm{G} \times \mathrm{I}+\mathrm{V}_{\mathrm{REF}}$, and the resistor equals $\left(\right.$ THRESHOLD $-V_{\text {REF }}$ )/G×I, where $G$ is the gain of the PGAA, $I$ is the desired current limit, and $\mathrm{V}_{\text {REF }}$ is the level-shifted reference voltage. For example, one application needs a 2 A overcurrentprotection limit, shunt resistor $R_{1}$ has a value of $0.02 \Omega$, and the PGA has a gain of eight. These values yield a currentthreshold voltage of $0.02 \Omega \times 8 \times 2 \mathrm{~A}=320$ $\mathrm{mV}+\mathrm{V}_{\text {REF }}=320 \mathrm{mV}+1.65 \mathrm{~V}=1.97 \mathrm{~V}$. You use an internal 8 -bit DAC to generate this voltage.
Implementing BLDC-motor control in hardware offers many benefits stem-
ming from the reduced processing requirement of the CPU. Hardware control leaves the CPU free for other sys-tem-processing tasks, reducing the peak processing requirements of the full motor system and resulting in lower system power and cost. It also makes the mo-tor-control design mostly autonomous and essentially a drag-and-drop function. It even makes it possible to control multiple independently operating motors with one microcontroller. This task requires high-performance microcontrollers without hardware commutation, which would cause two motors to simultaneously interrupt the CPU. This interruption would in turn cause one motor to see a delay in the updating of its PWM configuration if the response were too slow and would cause the motor to run unevenly. An 8-bit, 8051-based Cypress PSoC (programmable system on chip) 3 can control as many as six independent BLDC motors with sensors in hardware, leaving the microcontroller free to run other system tasks. The motors have independent hardware-commutation logic and fully independent speed control. Although this feature is possible without hardware commutation, it is not possible with an 8 -bit microcontroller because its response time is too slow. However, you need to implement firmware commutation if your application requires more advanced control algorithms, such as sinusoidal or field-oriented control.

Using a microcontroller to control both the motor and the user-interface functions can yield large cost savings.

Take, for example, an in-wall air-conditioning unit with a condenser motor, an air-blowing motor, and an oscillating air-direction motor. It also has buttons, a display, and an infrared remote control. Multiple microcontrollers on multiple boards previously would have had to perform most of these functions. With hardware commutation, however, one microcontroller could potentially integrate these functions, resulting in a major cost reduction. Some products cannot have a microcontroller controlling both functions, however, because the motor resides in a different location from the buttons or display.EDN

## AUTHORS' BIOGRAPHIES

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# NEW POWER REGULATIONS BRING POWER-FACTOR CORRECTION TO LOWER-POWER SUPPLIES 

BY MARGERY CONNER • TECHNICAL EDITOR

WITH THE INTRODUCTION
OF NEW POWER-SUPPLY SPECIFICATIONS FROM ENERGY STAR, COMPUTER POWER SUPPLIES AS LOW AS 75W AND SOLID-STATE LIGHTS AS LOW AS 5W MUST MEET MINIMUM POWER FACTORS, MAKING POWER FACTOR A CONCERN FOR MOST ELECTRONIC EQUIPMENT THAT USES AC-LINE POWER.

ntil recently, power factor and PFC (pow-er-factor-correction) circuits were of concern only for utilities and manufacturers of motors. Utilities have for years specified the power-factor performance of large inductive motors. The utilities also generally can charge industrial customers for reactive-power consumption. However, residential customers are starting to introduce more reactive-power loads into the mix as energy-efficient lights, such as CFLs (compact fluorescent lights) and LED-based lights containing their own ac/dc lighting ballasts, begin to emerge. As a result, power factor has moved from the realm of largescale industrial motors down to that of consumer electronics.

Power factor is the ratio of real power to apparent power. When both current and voltage are sinusoidal and in-phase, the power factor is one. If they are sinusoidal but not in-phase, then the power factor is the cosine of the phase angle. Purely sinusoidal current and voltage waveforms occur when the load comprises resistive, capacitive, and inductive elements that are all linear.

In a purely resistive load, real power is the same as apparent power, and the power factor is one. When the load has inductance or capacitance, however, the apparent power is less than the real power because the capacitance and inductance introduce a phase lag between
the current and the voltage. Although utilities currently charge residential customers only for the real power they consume, the utilities must add power to support the out-of-phase current and voltage. The additional power is wasted in the form of resistive losses on the grid's transmission lines. Because these losses increase as the square of the current increases, losses due to low power factor can quickly add up.

The ac line sees an SMPS (switchedmode power supply) as a nonsinusoidal, nonlinear impedance (Figure 1). Figure 2 shows the voltage and current for the circuit of Figure 1. To more closely follow the input voltage and avoid



Figure 1 The SMPS presents a nonlinear load to the ac-power line.
sharp current spikes, the capacitor must charge over the entire positive portion of the cycle. In addition to upping the power factor closer to one, this shaping of the current allows for the use of a smaller capacitor and avoids the creation of harmonic noise, thus reducing THD (total harmonic distortion). This compensating additional circuitry is the PFC circuit. Energy-efficiency specifications regulate both THD and power factor as part of the power-factor specification.

Note that PFCs decrease rather than increase power-supply efficiency. "Pow-er-supply designers are only moving to incorporating improved power factor in their supplies because of government mandates," says Steve Mappus,

## AT A GLANCE

Agencies such as Energy Star and Climate Savers are setting power factors for relatively lowpower consumer devices and computer servers.

PFC (power-factor correction) does not improve a supply's efficiency.

Digital PFC is becoming a costeffective design approach, especially for designs already containing a DSP or a microcontroller.
a systems engineer in the High Power Solutions group at Fairchild. The utility companies are the immediate beneficiaries of improved power factor, but consumers benefit downstream because utilities need not build additional power plants, holding pollution and carbon emissions in check.

Many topologies and approaches exist for enabling PFC (see sidebar "Utilities and PFC"). In general, PFC is either passive or active. Government and industry regulations specify only the power factor and the THD, leaving the

## TABLE 1 CLIMATE SAVERS CRITERIA <br> FOR MULTI-OUTPUT POWER-SUPPLY UNITS

|  | Bronze Level |  | Silver Level |  | Gold Level |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Loading <br> condition <br> $(\%)$ | Efficiency <br> $(\%)$ | Power <br> factor | Efficiency <br> $(\%)$ | Power <br> factor | Efficiency <br> $(\%)$ | Power <br> factor |
| 20 | 82 | 0.8 | 85 | 0.8 | 87 | 0.8 |
| 50 | 85 | 0.9 | 88 | 0.9 | 90 | 0.9 |
| 100 | 82 | 0.95 | 85 | 0.95 | 87 | 0.95 |

Source: Climate Savers, www.climatesaverscomputing.org/tech-specs
decision about whether to use a passive or an active circuit to the design engineer (tables 1 through 3 ).

Passive PFC is a simple, relatively inexpensive approach, but it has drawbacks. Chief among them is that it's difficult, although not impossible, to get a power factor of more than 0.7 , and the trend in global regulations is toward power factors of 0.9 and higher. Another difficulty with passive PFC is that the capacitors go directly on the ac line, necessitating capacitor ratings of 400 V or higher. This requirement makes the use of electrolytic capacitors the most common approach. Electrolytic capacitors' lifetime drops with higher temperatures, so you must derate the capacitor if your system will need to work in a hot environment. To derate it, you must either choose a higher temperature, more-expensive capacitor or allow for a shorter capacitor lifetime. Another drawback with passive PFC

## TABLE 2 LED-LIGHTING POWER-FACTOR CRITERIA

Equipment
Power factor
Solid-state-lighting luminaires

| Residential | $\geq 0.7$ |
| :---: | :---: |
| Commercial | $\geq 0.9$ |
| Integral LED lamps | $\geq 0.7$ |

## Sources:

http://www.energystar.gov/ia/partners/ prod_development/revisions/downloads/lighting/ESIntegralLamps Criteria_Draft1.pdf http://www.energystar.gov/ia/partners/ product_specs/program_reqs/SSL_ prog_req_V1.1.pdf

TABLE 3 ENERGY STAR POWER-FACTOR REQUIREMENTS
FOR COMPUTER-SERVER POWER SUPPLIES

|  |  | 10\% load |  | 20\% load |  | 50\% load |  | 100\% load |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Type | Rated output power | Power factor | Efficiency (\%) | Power factor | Efficiency (\%) | Power factor | Efficiency (\%) | Power factor | Efficiency (\%) |
| AC/DC multiouput | All output levels | NA | N/A | 0.8 | 85 | 0.9 | 88 | 0.95 | 85 |
| AC/DC singleoutput | <500W | NA | 80 | 0.8 | 88 | 0.9 | 92 | 0.95 | 88 |
|  | $\begin{aligned} & 500 \\ & \text { to } 1000 \mathrm{~W} \end{aligned}$ | 0.65 | 80 | 0.8 | 88 | 0.9 | 92 | 0.95 | 88 |
|  | >1000W | 0.8 | 80 | 0.9 | 88 | 0.9 | 92 | 0.95 | 88 |



Figure 2 Superimposing the current over the voltage for the circuit in Figure 1 shows the need for a PFC to shape the current.
is that its voltage output is unregulated as it feeds into the $\mathrm{dc} / \mathrm{dc}$-conversion stage. For these reasons, the trend is toward active PFC, usually in the form of a boost-converter circuit between the bridge rectifier and the storage capacitor.
The most common configurations for an ac/dc power supply with PFC are two-stage and single-stage designs. In a two-stage design, the ac line feeds into an ac/dc converter, usually comprising a bridge rectifier feeding into a capacitor whose output is usually full of sec-ond-harmonic ripple. A dc/dc converter follows the ac/dc converter to provide electrical isolation and voltage regulation. This approach keeps the two stages separate, is easy to troubleshoot, and is simple. However, the double conversion is less efficient, and costs are higher because of the need for two stages. As PFC becomes more prevalent, singlestage PFC is becoming more common.
Kishore Manghnani, vice president of Green Technology for Marvell, argues that single-stage power-converter/ PFC ICs are the best design approaches for LED lighting. "With two-stage you end up using two separate chips-one for PFC and the other for the LEDdriver circuit, which includes dimming and the TRIAC [triode-alternating-current-switch] interface," he says. "In a single-stage converter/PFC chip, you need no additional components: You put the LED driver and the PFC all in one chip." You might wonder whether you can use cheaper passive PFC, given that cost is a pacing item in LED lighting, but Manghnani advises against this approach. "The biggest advantage of active PFC is that you can use a lowvoltage capacitor," he says. "In passive PFC, the capacitor must support 400 V . In the active single-stage [approach], the capacitor is only 40 V . Plus, the life-
time of the capacitor [for the same cost] could be four to five times longer."

Currently, Energy Star's draft proposal for energy-efficient luminaires calls for a power factor of 0.7 in residential lighting and 0.9 in commercial, but Marvell argues that the power factor for LED lighting should be 0.9 for all lights with wattage higher than 5 W , which is currently the specification in Europe and Korea. "The United States is a bit behind in this area," Manghnani says. "Europe and Korea require lighting power to be more than 0.9. It doesn't cost anything extra, so why not add it?"
The mandate for minimum powerfactor requirements comes at the same time as the industry is imposing increasingly tight efficiency standards on power supplies, causing a double whammy on designers, who must strive for more stringent efficiencies as power factor creeps up. Thus, research is ongoing on the most efficient ac/dc-converter/PFC circuits. It's important to understand the general categories for control and which power-supply types these methods can work with. A brief overview of active-PFC methods follows. For more information and circuit diagrams, see references 1 and 2.
The main control methods for ac-tive-PFC circuits are DCM (discontin-uous-conduction mode), CCM (con-tinuous-conduction mode, and CRM (critical-conduction mode). Various chip manufacturers have their own versions of CRM control, such as BCM (boundary-conduction mode) and TM (transition mode). "Current conduction" in these terms refers to the inductor current.
Low-power supplies typically use DCM. CCM works for all power levels but involves a hard reverse recovery of the output diode when the MOSFET switch turns on. This recovery can

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cause high losses in a standard inexpensive diode. For high efficiency, therefore, you must use a more expensive diode, such as one made from silicon carbide.
In contrast, BCM circuits switch on the MOSFET with no current in the diode, allowing you to use inexpensive output silicon rectifiers. The trade-offs are that BCM uses a more complex variable-switching-frequency scheme, and its higher peak currents result in higher losses at higher power, limiting most BCM designs to less than 300W. At higher power levels, the CCM boost is more effective due to its lower ripple currents that result in lower peak currents and lower differential-mode EMI (electromagnetic interference).
However, recent innovations in converter/PFC design interleave multiple-

## UTILITIES AND PFC

According to Ken Lau, consulting engineer for PG\&E (Pacific Gas and Electric), a California electric utility, the utilities perform PFC (powerfactor correction) by switching in banks of capacitors at preset times. In a residential area, you can expect a surge in power use at about 7 a.m., so the substation automatically switches in a capacitor bank at that time, switching it out after $8 \mathbf{a} . \mathrm{m}$. No communication or real-time adjustment is necessary for this type of correction. In five to $\mathbf{1 0}$ years, however, many houses will have their own photovoltaic installations or perhaps even wind turbines, so the smart grid will be able to communicate with each house's power-subsystem inverter to perform PFC on the fly.
phase BCM-controller ICs, such as those from Fairchild, On Semiconductor, and Texas Instruments. Interleaved designs parallel two or more BCM power stages, allowing your design to reach 1 kW or more and reducing the ripple current in the output, which allows for smaller inductors. "If you look at the
costs of the controller in comparison to the costs of the PFC, which includes the inductor and all the power components, the controller is not a significant cost," says Jim Aliberti, product-marketing engineer at Texas Instruments. "It's the magnetics. People are looking for a way to reduce the costs, and inter-


CAN=CONTROLLER-AREA NETWORK
DALI=DIGITAL ADDRESSABLE-LIGHTING INTERFACE
$I^{2} \mathrm{C}=$ INTER-INTEGRATED CIRCUIT
SPI=SERIAL-PERIPHERAL INTERFACE
UART=UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER
Figure 3 A microcontroller performs PFC by controlling the current so that it is sinusoidal and in-phase with the input voltage. The TI C2000 uses one control loop at 100 kHz to keep this input current sinusoidal and uses a second, slower control loop to keep the output voltage stable. The C2000 has sufficient CPU bandwidth to perform this task and multiple others for the system.
leaved design has enabled lower system costs because you don't have to process as much ripple current, allowing you to use smaller magnetics."

As with most power-conversion applications, digital power is making inroads into PFC, as well. For example, Cirrus Logic offers an IC for digitally controlled PFC. The active-PFC CS1500 and CS1600 DCM ICs target use in power supplies requiring as much as 300W. The CS1500 addresses power supplies for applications such as laptops, digital TVs, and PCs, and the CS1600 targets electronic-lighting ballasts. At approximately 30 cents (high volumes), the chips compare in price with analog PFC ICs but use $30 \%$ fewer additional components and fewer parts for EMI filtering. The power factor, which varies with the input line voltage and the load, is greater than 0.95 . The iW3620 LED driver from iWatt is also a digital single-stage, active-PFC device. Texas Instruments offers a development kit for high-voltage PFC, which includes hardware and software to implement two-phase interleaved digital PFC for regulation compliance. The kit can work with the company's application-development kits for the C2000 Piccolo microcontrollers, such as the C2000 ac/dc developer's kit, as well as end-product kits, such as motorcontrol and LED-lighting-control kits.

Providing efficiency of as much as $30 \%$ in applications such as air conditioners and refrigerators, dc motors are replacing inductive motors in both residential and industrial applications. Because of their complex control algorithms, most dc-motor controllers use a DSP. Designers can add digital PFC to designs that already have a DSPoften with no additional components. The cost in engineering learning time

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can be considerable, though, which is why TI offers its DSP-developer kits for several applications. The digital-PFC kit can work to provide a PFC block for a DSP-motor controller. Another likely application for digital PFC is LED lighting. For example, a DSP such as the C2000 can run PFC in addition to powering an LED array (Figure 3).

Do you remember the advertising push several years ago for the smart refrigerator that would track when you were low on milk and autonomously order more? That idea didn't catch on. Perhaps the more likely intelligence will be a DSP that controls all of the power-efficient function of home appliances.EDN

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# Architecture combines low- and zero-IF receivers 

## A SWITCH-MATRIX MIXER PROVIDES THE DOWNCONVERSION FUNCTION IN THIS NOVEL RADIO.

ow-IF (intermediate frequen-cy)-receiver architectures are increasingly popular for many wireless standards. You can detect the signal at the IF or downconvert it to baseband after the ADC stage. This circuit does the final downconversion using a switch-matrix mixer before the analog-to-digital conversion. You use analog filters following the mixer stage. This approach reduces the dynamic range the following ADC stage requires. By doing simulations and taking measurements on a prototype, you can investigate the effect of nonideal switches in the matrix.
Before delving into the details, you should understand the history of this architecture. The superheterodyne receiver has for decades been the architecture of choice because it provides excellent receiver properties, such as selectivity and sensitivity. The architecture does not easily lend itself to integration, however, because you must implement the image-rejection filters in a discrete circuit.
Direct-conversion, or zero-IF, receivers have recently gained importance (Reference 1). This architecture is appropriate for integration, but it causes other problems. A direct-conversion architecture has dc-offset problems that necessitate a dc-nulling strategy (references 2 and 3). In body-worn radio equipment, the antenna's impedance matching changes frequently. In this case, it is difficult to build a wellbehaved dc-nulling circuit. Furthermore, modern high-speed modulation schemes must have a continuous baseband spectrum without gaps.
To avoid this problem, you can build low-IF, or quasi-direct-conversion, receivers (Reference 2). The desired signal bandwidth after a low-IF-conver-
sion step is on either the positive- or the negative-frequency side, but it does not include any dc part of the spectrum. You can then ac-couple the subsequent ADC.

The final downconversion to baseband usually takes place in the digital domain. You multiply the complex signal with a rotating phasor. Choosing a low IF that is one-quarter of the sampling frequency eases these operations by reducing the number of multiplications to those for swapping samples and changing their signs every other time.
To illustrate this approach, you denote the incoming signal at low IF as $\mathrm{s}(\mathrm{t})$ and mix down the signal with frequency $f_{\text {LO }}$ (Equation 1):

$$
\begin{equation*}
\tilde{s}(\mathrm{t})=\mathrm{s}(\mathrm{t}) \times \mathrm{e}^{-\mathrm{j} 2 \pi f_{\mathrm{LO}} \mathrm{t}} . \tag{1}
\end{equation*}
$$

You then sample Equation 1 with a sampling frequency $f_{S}$ of $1 / T_{S}$ :

$$
\tilde{\mathrm{x}}(\mathrm{t})=\sum_{\mathrm{k}=-\infty}^{\infty} \mathrm{s}\left(K T_{\mathrm{S}}\right) \times \mathrm{e}^{-\mathrm{j} 2 \pi f_{\mathrm{L}} k T_{\mathrm{S}}}
$$

You choose $\mathrm{f}_{\mathrm{LO}}$ to satisfy Equation 3:

$$
\begin{equation*}
\mathrm{f}_{\mathrm{LO}}=\frac{\mathrm{f}_{\mathrm{S}}}{4}=\frac{1}{4 \mathrm{~T}_{\mathrm{S}}} \tag{3}
\end{equation*}
$$

Equation 2 then results in Equation 4:

$$
\begin{gather*}
\tilde{\mathrm{x}}(\mathrm{t})=\sum_{\mathrm{k}=-\infty}^{\infty} \mathrm{s}\left(\mathrm{k} \mathrm{~T}_{\mathrm{S}}\right) \times \mathrm{e}^{-\mathrm{j} \frac{\pi}{2} \mathrm{k}} \\
=\sum_{\mathrm{k}=-\infty}^{\infty} \mathrm{s}\left(4 \mathrm{k} T_{\mathrm{S}}\right)-\mathrm{j} \sum_{\mathrm{k}=-\infty}^{\infty} \mathrm{s}\left((4 \mathrm{k}+1) \mathrm{T}_{\mathrm{S}}\right) \\
-\sum_{\mathrm{k}=-\infty}^{\infty} \mathrm{s}\left((4 \mathrm{k}+2) \mathrm{T}_{\mathrm{S}}\right)+\underset{\mathrm{j}=-\infty}{\infty} \sum_{\mathrm{k}=-\infty}^{\infty}\left((4 \mathrm{k}+3) \mathrm{T}_{\mathrm{S}}\right) \tag{4}
\end{gather*}
$$

If you represent signal $s(t)$ in its I/Q (inphase/quadrature) form as a real and an
imaginary part, you can rewrite Equation 4 as Equation 5:

$$
\begin{gather*}
\tilde{\mathrm{x}}(\mathrm{t})=\sum_{\mathrm{k}=-\infty}^{\infty}\left[\operatorname{Re}\left(\mathrm{s}\left(4 \mathrm{k} \mathrm{~T}_{\mathrm{S}}\right)\right)+\right. \\
\sum_{\mathrm{k}=-\infty}^{\infty} \operatorname{Im}\left(\mathrm{s}\left((4 \mathrm{k}+1) \mathrm{T}_{\mathrm{S}}\right)\right)- \\
\sum_{\mathrm{k}=-\infty}^{\infty} \operatorname{Re}\left(\mathrm{s}\left((4 \mathrm{k}+2) \mathrm{T}_{\mathrm{S}}\right)\right)- \\
\left.\sum_{\mathrm{k}=-\infty}^{\infty} \operatorname{Im}\left(\mathrm{s}\left((4 \mathrm{k}+3) \mathrm{T}_{\mathrm{S}}\right)\right)\right] \\
+\mathrm{j}\left\{\sum _ { \mathrm { k } = - \infty } ^ { \infty } \left[\operatorname{Im}\left(\mathrm{~s}\left(4 \mathrm{k} \mathrm{~T}_{\mathrm{S}}\right)\right)-\right.\right. \\
\sum_{\mathrm{k}=-\infty}^{\infty} \operatorname{Re}\left(\mathrm{s}\left((4 \mathrm{k}+1) \mathrm{T}_{\mathrm{S}}\right)\right)- \\
\sum_{\mathrm{k}=-\infty}^{\infty} \operatorname{Im}\left(\mathrm{s}\left((4 \mathrm{k}+2) \mathrm{T}_{\mathrm{S}}\right)\right)+ \\
\left.\left.\sum_{\mathrm{k}=-\infty}^{\infty} \operatorname{Re}\left(\mathrm{s}\left((4 \mathrm{k}+3) \mathrm{T}_{\mathrm{S}}\right)\right)\right]\right\} . \tag{5}
\end{gather*}
$$

This form represents the switching function. The major drawback of this technique is if only real analog filters are applied before the analog-to-digital conversion, the ADCs must have a high dynamic range. Wireless-communication equipment has adjacent-channel rejection on the order of 70 dB . In this case, the adjacent channel is the image frequency corresponding to the negative frequency of the desired signal. The ADC must provide more than 12 bits of dynamic range, including the possible signal dynamics of nonconstant envelope-modulation schemes. These ADCs are expensive, and they consume a lot of power.

A possible approach is to apply polyphase filters, which can separately filter the negative and positive frequencies (Reference 4). This approach increases the circuit's complexity for a given order of filters because the coefficients of such filters are both real and imaginary.


Figure 1 A switch-matrix mixer changes a low-IF architecture into a zero-IF receiver.

Downconverting the signal from low IF to zero IF before filtering and analog-todigital conversion eliminates the need for polyphase filters and still uses an ADC with reduced dynamic range.

## ARCHITECTURE AND CIRCUIT

You can use switches as mixers in downconversion architectures by assuming that you have both the inverse and the noninverse of the real and imaginary parts of the signal (Reference 5). The switch-matrix mixer comprises eight switches operating in four phases that feed the four signals, $\mathrm{I}+, \mathrm{I}-, \mathrm{Q}+$, and $Q-$, to the input of a subsequent filter. You can implement the matrix with transmission-gate FET switches. The equivalent operation of these switches is mixing by one-fourth of the sampling frequency (Equation 6):

$$
\begin{equation*}
\mathrm{f}_{\mathrm{LO}}=-\frac{\mathrm{F}_{\mathrm{S}}}{4} \tag{6}
\end{equation*}
$$

You insert the switch matrix into the receiver chain (Figure 1). The num-
bers assigned to the switches denote the phases when they are closed. You drive the switches with phase-shifted signals (Figure 2). The switching function, $G(t)$, applies the mixing process to signal $\mathrm{s}(\mathrm{t})$ (Equation 7):

$$
\begin{equation*}
\tilde{s}(t)=s(t) \times G(t) \tag{7}
\end{equation*}
$$

The switching function, $G(t)$, has some harmonics, requiring you to apply some filtering after the mixing process (see sidebar "Fourier coefficients of a switch-matrix mixer," available with the Web version of this article at www. edn.com/ms4373). You can combine this filter with the ADC's antialiasing filter.

A low-IF-receiver architecture has adjacent channels in the negative-frequency range of the desired signal (Figure 3). A real antialiasing filter can filter out only adjacent Channel 2. Adjacent Channel 1 is the image of the desired channel and passes through the antialiasing filter without attenuation. The antialiasing filter must be good enough to prevent aliasing from adjacent Channel 2. The ADCs require a dynamic range greater than 70 dB .
The addition of the switch-matrix mixer moves the desired signal into the baseband (Figure 4). The antialiasing filter must filter out not only the adjacent channels but also the mixing terms from

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Figure 3 The spectrum of a low-IF system may have strong adjacent channels. Here, $f_{S}$ denotes the sampling frequency; $f_{N}$, the Nyquist frequency; and $\mathrm{f}_{\mathrm{L} \text {, }}$, the low IF.
the harmonics of the switching function. In this case, however, the antialiasing filter's bandwidth is half that of the previous case. Maintaining the same filter order results in a sharper antialiasing filter. The filter suppresses both adjacent channels, dramatically reducing the ADC's required dynamic range.
Other channels outside the adjacent channels may fall into the baseband due to mixing with the harmonics of the switch function. To address this problem, you must apply an image filter in front of the switch-matrix mixer. This filter is more relaxed than the antialiasing filter. Both adjacent channels are filtered, so the antialiasing filter allows the ADC to have a lower number of bits.

## SIMULATION RESULTS

You can do a simulation using The MathWorks (www.mathworks.com) Matlab to illustrate the process of an ideal low-IF mixer (Figure 5). You can simulate a $100-\mathrm{kHz} \mathrm{RF}$ signal with a strong interferer at 70 kHz . The spectrum at this point is symmetric, corresponding to a real signal. A complexvalued mixer shifts down the signal to the low IF, making the spectrum asymmetric. An interferer signal appears at the image frequency with respect to zero. Derotating with the remaining IF yields a zero-IF baseband signal. You can filter away the interferer using a real-valued filter.
You can also simulate an ideal switchmatrix mixer (Figure 6). The first two plots are the same as those in Figure 5 because the switch-matrix mixer replaces only the low-IF derotation process. The third plot depicts that, even with perfect switches, some spectral interleaving occurs. You can separate these


Figure 4 A switch-matrix mixer shifts the spectrum to zero-IF but also adds switching Fourier components to the adjacent channels.

IF signal to the test board. It downconverts the signal to a baseband signal using a clock frequency of four times 14 kHz to get four phases, resulting in 56 kHz . After the first mixing process, the resulting frequency spectrum of this signal has three peaks
interlaced higher-order products using filtering, as the bottom plot shows. Introducing a gain error causes even more spectral interleaving (Figure 7). These additional subbands are filtered off and do not cause a problem. However, I/Q imbalance results in the usual image problem, quantitatively of the same order as with any low-IF mixer.

A prototype PCB (printed-circuit board) of the switch-matrix mixer includes the clock-phase generators (Figure 8). Lowpass filters surround the switch-matrix mixers. You mix a $2.40002-\mathrm{GHz} \mathrm{RF}$ signal, which is 20 kHz offset from 2.4 GHz , with a $20-\mathrm{kHz}$ IF using a Maxim (www.maxim-ic.com) MAX2701 image-rejection mixer. You send the I and the Q part of the low-
(Figure 9). One peak is the image at -20 kHz , or 40 dB down. The second peak is the dc offset. The third peak is the signal of interest at 20 kHz .
After the second mixing process, the signal of interest now shifts to 6 kHz (Figure 10). The previous dc peak shifts to -14 kHz , and the switch-matrix mixer generates a new dc-offset peak; 40 dB also suppresses the image of the switchmatrix mixer at -6 kHz . Choose the cutoff frequencies of the lowpass filters before and after the switches as 30 and 15 kHz , respectively.

A switch-matrix mixer reduces the dynamic range needed in a subsequent ADC. Apart from the switches, only an additional low-order filter is necessary to prevent unwanted harmonics from fall-


Figure 5 Using ideal mixers, you can move the spectrum to a zero-IF baseband. Starting with an RF signal and a strong interferer (a), the first conversion makes the low-IF signal (b). Derotation moves the desired signal to the baseband (c), and filtering removes the unwanted negative-frequency components (d).


Figure 6 A switch-matrix mixer using ideal switches can also make a zero-IF signal. Starting with an RF signal and a strong interferer (a), the first conversion creates the low-IF signal (b). The switch-matrix mixer moves the signal to the baseband (c). Filtering removes the unwanted frequency components (d).


Figure 7 A switch-matrix mixer with a gain error in the signal chain exhibits problems.
The RF signal and strong interferer (a) move to low IF (b). The gain error causes worse interleaving (c). The filtered signal has typical image problems due to I/Q imbalance (d).


Figure 8 You can fabricate a hardware test board for a switched-matrix-mixer proof of concept.


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Figure 9 The input spectrum to the test board has the desired signal of 20 kHz .


Figure 10 The spectrum at the output of the switch-matrix mixer moves the desired signal to 6 kHz .
ing into the baseband. You can integrate these functions into a single IC.EDN

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## AUTHOR'S BIOGRAPHY

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## Control a dc motor with your PC

Firas M Ali Al-Raie,
Polytechnic Higher Institute of Yefren, Yefren, Libya

VThe circuit in this Design Idea controls the speed of a 5 V perma-nent-magnet dc motor through the PC's parallel port (Figure 1). You use the $\mathrm{C}++$ computer program, available at www. edn.com/100826dia, to run the motor at three speeds. The circuit uses PWM (pulse-width modulation) to change the average value of the voltage to the dc motor. You connect the motor to the PC's parallel port with an interface circuit. The design comprises $\mathrm{IC}_{1}$, a 74LS244 buffer; $\mathrm{IC}_{2}$, a ULN2003 driver; relay switches $\mathrm{S}_{1}, \mathrm{~S}_{2}$, and $\mathrm{S}_{3} ; \mathrm{IC}_{3}$, a 555 astable multivibrator circuit; and $Q_{1}$, a 2N2222 driving transistor. The 555 timer
operates as a variable-pulse-width generator. You change the pulse width by using relays to insert or split resistors in the 555 circuit.
The computer program controls these resistors. When $S_{1}$ is on and both $S_{2}$ and $\mathrm{S}_{3}$ are off, the timer output is set to logic one, thereby driving the motor with its maximum speed. When $S_{1}$ and $S_{2}$ are on, the 555 timer generates a pulse signal with a $50 \%$ duty cycle. In this case, the charging resistor, $\mathrm{R}_{\mathrm{A}_{1}}$, is equal to the discharging resistor, $\mathrm{R}_{\mathrm{B}}$. In the third case, $\mathrm{S}_{1}$ and $\mathrm{S}_{3}$ are on, and the charging resistor is $R_{A 2}$, where $R_{A 2}=0.1 \times R_{B}$, reducing the on time of the pulse signal and,

## DIs Inside

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47 LED indicates power source

- To see all of EDN's Design Ideas, visit www.edn.com/designideas.
consequently, the speed of the motor to the lower limit. Table 1 summarizes the on/off-operation conditions of the relays and the corresponding dc-motor speeds.


Figure 1 This circuit controls the speed of a 5 V permanent-magnet motor through the PC's parallel port.

## designideas

The code prompts you to select a certain speed, stores your selection as an integer variable choice, generates the proper digital sequence, and stores it at another integer variable. You place the value of the integer variable data at a PC's parallel port using the outportb function. The program uses the kbhit function to stop the motor when you hit any key on the keyboard.EDN

## SWITCH STATES AND GENERATED PC SEQUENCES

| $\mathbf{S}_{3}$ | $\mathbf{S}_{2}$ | $\mathbf{S}_{1}$ | Equivalent <br> digital sequence | Motor speed |
| :---: | :---: | :---: | :---: | :---: |
| Off | Off | Off | 000 | Stop |
| Off | Off | On | 001 | Maximum |
| Off | On | On | 011 | Medium |
| On | Off | On | 101 | Minimum |

# Look-up table eliminates the need for an IC 

Abel Raynus, Armatron International, Malden, MA

When you need to connect a
ment LED display, you can use a BCD (binary-coded-decimal)-to-seven-seg-


Figure 1 A CD4511 converts BCD codes to seven-segment-displays.


Figure 2 The look-up table lets the microcontroller produce a seven-segment output.
ment decoder. Figure 1 shows a typical circuit that uses a CD4511 to translate a 4-bit code into BCD.

Unfortunately, a limited size and budget may force you to omit components whenever possible. This requirement is especially critical with consumer products. Simple firmware allows you to overcome this limitation by directly connecting the display to a microcontroller (Figure 2).

A recent project used the 8 -bit Freescale (www.freescale.com) MC68HC-

> A NUMERIC DISPLAY NEEDS A SPECIAL SEVEN-SEGMENT CODE, THE VALUE OF WHICH DEPENDS ON THE COMMON POINT OF THE DISPLAY LEDs.

908QY4 microcontroller. When you write code for a microcontroller, you often represent data in decimal, hexadecimal, or BCD formats. A numeric display needs a special seven-segment code, the value of which depends on the common point of the display LEDscommon cathode or common anodeand on microcontroller outputs you choose for display. Tables 1 and 2 show how to obtain seven-segment code values for common-cathode and commonanode displays, respectively.

No mathematical connection exists between seven-segment code and any of these formats. Thus, you must use a table that a previous Design Idea

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Small

| Part | Watchdog Timer | Reset Output | Package |
| :---: | :---: | :---: | :---: |
| MAX16056 | $\checkmark$ | Push-pull | 8-TDFN |
|  | MAX16057 |  |  |
| 6-TDFN |  |  |
| MAX16058 | $\checkmark$ | Open drain | 8-TDFN |
|  | MAX16059 |  |  |

## www.maxim-ic.com/MAX16056-9-info

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## designideas

| CODE FOR COMMON-CATHODE DISPLAY |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Decimal number | $\mathrm{pB7}$ | pB6 <br> (g) | $\underset{\substack{\text { (f) }}}{\substack{\text { PB5 }}}$ | pB4 (e) | pB3 (d) | pB2 (c) | pB1 <br> (b) | pBO (a) | Sevensegment code |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | \$3f |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | \$06 |
| 2 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | \$5b |
| 3 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | \$4f |
| 4 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | \$66 |
| 5 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | \$6d |
| 6 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | \$7c |
| 7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | \$07 |
| 8 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | \$7f |
| 9 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | \$6f |

CODE FOR COMMON-ANODE DISPLAY

| Decimal number | pB7 - | pB6 <br> (g) | $\begin{gathered} \text { pB5 } \\ \text { (f) } \end{gathered}$ | pB4 <br> (e) | pB3 <br> (d) | $\begin{array}{\|l\|} \hline \text { pB2 } \\ \text { (c) } \end{array}$ | pB1 <br> (b) | pBO <br> (a) | Sevensegment code |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | \$40 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | \$79 |
| 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | \$24 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | \$30 |
| 4 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | \$19 |
| 5 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | \$12 |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | \$03 |
| 7 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | \$78 |
| 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | \$00 |
| 9 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | \$10 |

describes (Reference 1). The project described here used one seven-segment LED display to show the digits 0 through 9. A table makes the firmware simple and short.
Using the assembly-language code that you can download from the online version of this article at www.edn. com/100826dib, you need just 7 bytes

> A DECIMAL NUMBER FOR CONVERSION GOES INTO A REGISTER AND ACTS AS AN INDEX APPLYING TO THE CODE TABLE.

to execute the program, plus 10 bytes of memory for the code table. A decimal number for conversion goes into register DECreg and acts as an index, X , applying to the code table. The result appears at the microntroller's Port B output.EDN

## REFERENCE

TRaynus, Abel, "Tables ease microcontroller programming," EDN, April 22, 2010, pg 76, www.edn.com/ article/457500-Tables_ease_
microcontroller_programming.php.

## Operate circuits at voltages as high as 540 V ac

Vipin Bothra and John Lo Giudice, STMicroelectronics, Schaumburg, IL



Energy meters, HVAC (heating/ ventilation/air-conditioning) systems, and high-power equipment that runs on three-phase ac inputs pose a challenge to power-supply designers because nominal input voltage can be as high as 540 V ac. The challenge increases if the power supply must operate from 100 to 540 V ac. Design choices are numerous, and final system costs can vary dramatically with those choices. An abundance of parts is available for power supplies with input power as high as

240 V ac. High-voltage input-power supplies are, however, still a niche area for most semiconductor companies.
The power-supply circuit in Figure 1 uses an input-chopper circuit that allows the clamping of input voltage to the flyback power stage so that the power is less than 400 V . That voltage lets you use a standard design technique for the flyback stage. The input chopper provides many advantages over prevailing high-voltage-input power supplies.
Unlike a standard flyback converter,
this circuit eliminates the need for a high-voltage MOSFET for the switch, thereby letting you use lower-cost, commonly available MOSFETs. Moreover, overall switching losses in the power supply decrease dramatically with the reduction in bus voltage. The circuit can use smaller and lower-cost transformers because of a reduction in creepage-clearance requirements.
This circuit's reduced bus voltage eliminates the stacked-FET-flyback topology and the need for two or more high-voltage capacitors. It also improves the overall efficiency of the system by eliminating the high losses of a stacked FET, replacing them with small losses from a bypass switch.


Figure 1 A chopper circuit reduces power-bus voltage to less than 400 V dc per pin.

The $500 \mathrm{~V}, 2.7 \Omega$ STP4NK50Z Nchannel MOSFET switches at the line frequency. It turns on at a predetermined voltage, and it turns off at any higher voltage. It limits the voltage on $\mathrm{C}_{2}$ to approximately 360 V dc. When the voltage at the divider of $R_{2}$ and $R_{4}$ reaches approximately 6.3 V , or 360 V at the top of the divider, $Q_{1}$ turns on and steals cur-

THE 500V MOSFET TURNS ON AT A PREDETERMINED VOLTAGE; IT TURNS OFF AT ANY HIGHER VOLTAGE.
rent from the gate of $Q_{2}$, and the MOSFET turns off. The divider sets the level at which $Q_{2}$ switches. All resistors are 0.25 W except for $\mathrm{R}_{\text {, }}$, which can be 2 W to survive surge. The circuit underwent testing with 12 W of output power at 90 to 440 V -ac input. The maximum input current to the power supply depends on the thermal performance of $Q_{2}$.EDN

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## Microcontroller supervises 0 - to $20-\mathrm{mA}$ protection circuit

Anatoly Andrusevich, Maxim Integrated Products, Moscow, Russia

$\triangle$
The 0 - to $20-\mathrm{mA}$ current loop is a reliable means of data communication in industrial applications. These circuits use a precision shunt in the receiver to convert the current signal into a voltage signal. Accidentally connecting the precision shunts to the current-loop power supply can cause damage, after which you must replace
the shunt and recalibrate the system. To avoid that expense, you can use a microcontroller-controlled protection circuit (Figure 1).

With conventional techniques, you protect the shunt with a fast fuse or by turning off the loop with an automatic switch, which then turns back on after a specified period. The circuit
in Figure 1 provides protection that is much faster than a fuse. $\mathrm{IC}_{1}$, the slowest device in the circuit, switches off in less than $500 \mu \mathrm{sec}$. It offers a high-er-precision switching threshold than a fuse, and, of course, there's no fuse to replace. Rather than making you cycle power to restore the loop, the microcontroller provides control of the protection circuit. The microcontroller also logs the event, thereby providing a record that the system invoked the protection circuit.

The protection circuit has virtually


Figure 1 This circuit protects the isolated analog front end of a current loop. For simplicity, the drawing omits power and ground connections for $\mathrm{IC}_{2}, \mathrm{IC}_{4}, \mathrm{IC}_{5}$, and $\mathrm{IC}_{6}$.
no effect on the analog front end. The $\mathrm{IC}_{2}$ buffer ensures an input current of less than 30 pA . The on-resistance of $\mathrm{IC}_{1}$ is less than $2 \Omega$. The circuit needs no additional isolated data channels or microcontroller-I/O ports, and it prevents damage during system installation or repair. It also turns off the loop after power-up and when no power is available.
You implement the protection algorithm with a power-fail comparator and a watchdog circuit, available as separate outputs on $\mathrm{IC}_{3}$, together with $\mathrm{IC}_{6}$, a D type flip-flop.
At power-up, the flip-flop is in the reset state, and the current loop is open,

## THE CIRCUIT NEEDS NO ADDITIONAL ISOLATED DATA CHANNELS, AND IT PREVENTS DAMAGE DURING SYSTEM INSTALLATION.

due to a high-level reset signal from $\mathrm{IC}_{3}$ driving $\mathrm{IC}_{4}$, a NOR gate. After the first low-to-high transition on the SCK (clock-signal) line, a rising edge from
$\mathrm{IC}_{3}$ 's $\overline{\mathrm{WDO}}$ (watchdog output) sets the flip-flop and pulls current through the solid-state relay, $\mathrm{IC}_{1}$, thus connecting the input to the loop.
In the event of a loop-current overload greater than 27 mA , a high level from the $\overline{\mathrm{PFO}}$ (power-fail-output) comparator on $\mathrm{IC}_{3}$ resets the flip-flop and switches off $\mathrm{IC}_{1}$. Thanks to the $\mathrm{IC}_{5}$ gate, the microcontroller inputs ones at the MISO (master input/slave output), meaning overcurrent.
To again switch on the loop, the micro controller must stop the SCK line for at least 2.4 sec . The next low-to-high transition on SCK then reconnects the current loop.EDN

## LED indicates power source

Brian Conley, Circuitsville Engineering LLC, Beaverton, OR

घLED circuits with current-limiting resistors find extensive use as power indicators and for debugging circuits (Reference 1). In some cases, however, your design may require a different approach. Bipolar transistors have a lit-tle-discussed behavior: reverse active region. For low voltages and small currents, an NPN transistor can operate in reverse with a significantly lower gain,

## THE LED ILLUMINATES WHEN THE BOARD RECEIVES VOLTAGE FROM THE WALL WART, BUT NOT FROM THE USB PORT.

which can be undesirable. Some linear regulators also operate in this way.
The circuit in Figure 1 gets its inputvoltage power primarily from a wallwart dc-power supply that can provide 7 to 12 V . It may also get 5 V from a USB (Universal Serial Bus) port. This design requires a circuit that indicates whether the board is receiving voltage from the wall wart or from the USB port.

The circuit uses $\mathrm{Q}_{1}$, a 2 N 7002 FET, and zener diode $\mathrm{D}_{1}$ to solve the problem. The FET is in series with LED $_{1}$ and current-limiting resistor $\mathrm{R}_{1}$. Diode $\mathrm{D}_{1}$ is a Vishay (www.vishay.com) AZ23C4V3-V, which has a typical reverse voltage of 4.3 V within a range of 4 to 4.6 V . When $Q_{1}$ 's gate-to-source voltage exceeds its threshold-voltage range of 1 to 2.5 V , the LED turns on. The voltage coming from the USB port is insufficient to turn on $\mathrm{LED}_{1}$ because of the voltage drop across $D_{1}$. Thus, the LED illuminates when the board receives voltage from the wall wart, but not from the USB port.
Under testing, the LED illuminates when the input voltage is at least 7.1 V . When it is below that voltage, the LED is off, indicating that the USB port is powering the circuit.
Resistor $\mathrm{R}_{3}$ comprises two $1-\mathrm{k} \Omega$ resistors in parallel. This setup is necessary because the input voltage is 12 V and the zener diode's minimum voltage is 4 V . A voltage of 8 V appears across $\mathrm{R}_{3}$, producing 0.128 W -too much power for one resistor in a 0805 package.EDN

## REFERENCE

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Figure 1 This circuit gets its power from a wall-wart dc-power supply or from a USB port. The LED illuminates when the board receives its voltage from the wall wart. When it is off, the USB port is powering the circuit.

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Orion Fans, www.orionfans.com

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Tortran Inc, www.tortran.com

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## Bud Industries Inc, www.budind.com

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Nuventix Inc, www.nuventix.com

## SWITCHES AND RELAYS

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## Fairchild Semiconductor,

www.fairchildsemi.com

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## AVTECH

## DAC days, sleepless nights



Afew years ago, I was working on a drive board for a thermal-radiation-sensor array that required testing. The serially multiplexed sensor output needed a multistep closed-loop correction scheme to even out sensor nonuniformity.

To perform the test, I employed a design with a dual serial DAC. I coded the software for the correction scheme, and it was then time to check out the operation. I decided to look at the DAC chip and its operation independently of the other components. I hooked up a board with the DAC to the microcontroller controlling the operation. To verify the controller's output, I used an oscilloscope that was monitoring the serial signal arriving at the DAC. It checked out fine and met all the parameters that the DAC manufacturer had set.

However, the analog output from the DAC was incorrect. At start-up, one DAC channel read 200 mV , and the other read 5 V . After the DAC received the data packet, the outputs read 0 and 5 V . Suspecting some software issue that I had overlooked, I spent an entire
afternoon going over the details of the correction scheme and the serial data packet's transmission to the DAC from the controller. I also checked the connections and wiring to the DAC and found everything to be correct.

The DAC chip was a new unit, and I did not consider it a likely suspect. After much hair pulling and teeth gnashing, nothing fruitful emerged. In frustration, I gave up for the day, hoping that the next day would yield some clue.

Sleep that night was elusive. I kept having visions of how the serial-packet transmission matched the timing diagram on the DAC manufacturer's data sheet. The power supply checked out, the hardware wiring checked out, and the software checked out. What else was left to check? By all accounts, the DAC should have behaved correctly. Maybe it
was a faulty chip after all. These thoughts occupied my sleepless night until the next morning, when I headed back to the lab.

I removed the DAC board from the controller and powered it up. The DAC had a power-on-reset feature that should have zeroed the DAC outputs at startup, but this feature did not seem to be working. One channel was still 5 V , and the other was still about 200 mV . When the DAC received the serial packet of data from the controller, the $200-\mathrm{mV}$ channel would drop to 0 V , and the other one remained at 5 V . I verified the serialpacket data again and found it to be correct. I carefully checked the wiring of the DAC and the serial connection and found nothing wrong. It looked indeed as if the chip was faulty.

Unfortunately, I seemed to have run out of parts to try a replacement. Loathing the thought of more sleepless nights until I solved the problem, I rummaged through my parts bin, hoping desperately to find another chip to test. Lo and behold, there at the corner of my bin was one last remaining DAC chip. Eagerly grabbing the part, I got ready to replace the chip on the board. This chip was a DIP, and I used an extractor to remove the suspicious chip from the board.

As I closely examined the chip and positioned the extractor on it, I was shocked to find that the faded partnumber marking showed that it was not a DAC chip at all but a dual op amp! I was doing all my testing with the wrong part in the socket! Cursing myself and thanking my lucky stars that I didn't blow anything else, I wrenched it out and replaced it with the correct part, hooked up the controller, and found that everything worked like a charm.

As one version of Murphy's Law states, "When you have removed the last of the 40 screws holding down an access door, you will find that you have removed the wrong access door." My sleep that night was indeed satisfying.EDN

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- Input Voltage: 4.5 V to 38 V
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- Powerful $1.5 \Omega$ Gate Drivers
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- LTC3787: 2-Phase Single Output

Minimal Temp Rise in the MOSFETs No Heatsink or Air Flow


1, $2,3 \& 4$ are Top and Bottom MOSFETs $V_{\text {IN }}=9 V, V_{\text {OUT }}=12 V, I_{\text {OUT }}=8 \mathrm{~A}(96 \mathrm{~W})$ Max Temp Rise $=43.7^{\circ} \mathrm{C}$

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[^0]:    The Xperia X10 mini offers IEEE 802.11b/g Wi-Fi as another wireless-connectivity option. Fueling all of the circuitry is a 3.7V, 950-mAhr lithium-polymer battery, which users cannot remove. Like the battery in Apple's iPhone 3GS, the Xperia's battery delivers approximately 53-mAhr/gram storage capacity.

[^1]:    Visit the Mechatronics Zone for the latest mechatronics news, trends, technologies, and applications at http://bit.ly/kor7L.

